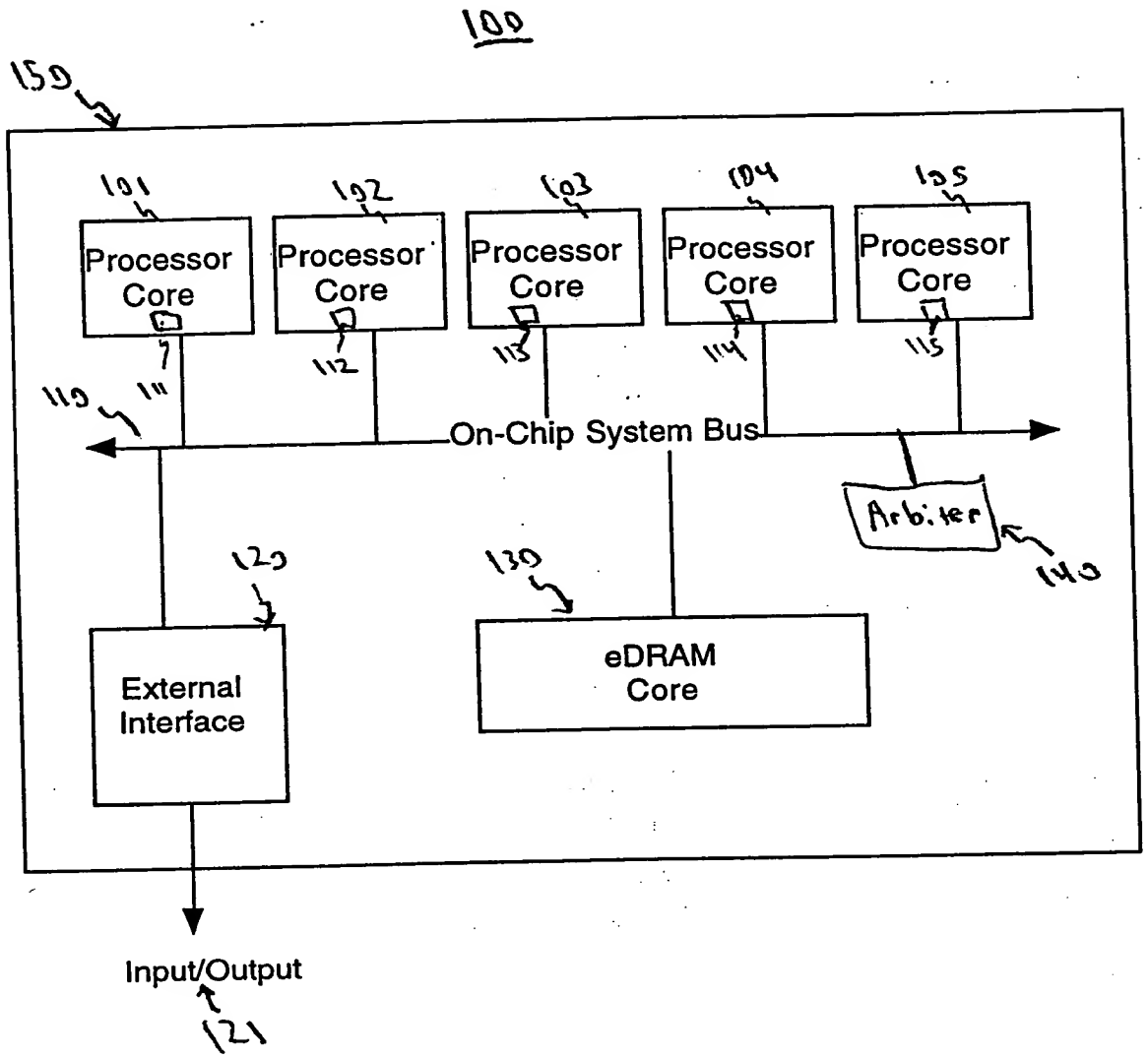
100
150
101
102
103
104
105
Processor Core
Processor Core
Processor Core
Processor Core
Processor Core
111
112
113
114
115
110
On-Chip System Bus
Arbiter
140
120
130
External Interface
eDRAM Core
Input/Output
121

FIG. 1

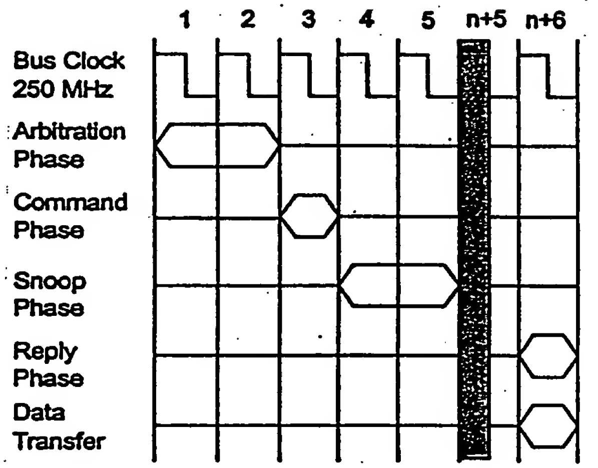
1
2
3
4
5
n+5
n+6
Bus Clock 250 MHz
Arbitration Phase
Command Phase
Snoop Phase
Reply Phase
Data Transfer

Fig 2

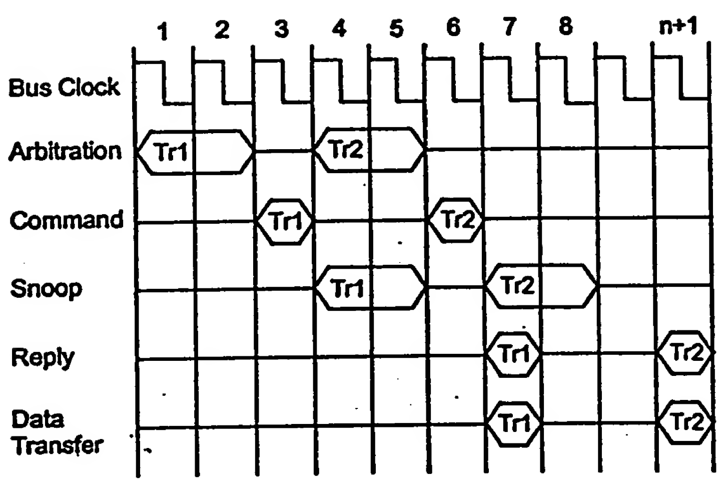
1
2
3
4
5
6
7
8
n+1
Bus Clock
Arbitration
Command
Snoop
Reply
Data Transfer
Tr1
Tr2

Fig. 3

Signal Function	Signal Name	Signal Direction[a]	Number of Signals
Global Bus Control Signals			
Bus Clock	OcsbClk	Input	1
Initialization	OcsbReset, OcsbInit	Input	2
Flush	OcsbFlush	Input	1
Arbitration Phase Signals			
Processor Agent Bus Request	OcsbProcBusReq[3:0]	Output	4
Memory or I/O Agent Bus Request	OcsbMemIOBusReq	Output	1
Processor Agent Bus Grant	OcsbProcBusGrant[3:0]	Input	4
Memory or I/O Agent Bus Grant	OcsbMemIOBusGrant	Input	1
Command Phase Signals			
Address Strobe	OcsbAddrStrb	Bidirectional	1
Command	OcsbCmd[3:0]	Bidirectional	4
Address	OcsbAddr[35:0]	Bidirectional	36
Snoop Phase Signals			
Hit a Shared State Cache Line	OcsbHitShrd	Bidirectional	1
Hit a Modified State Cache Line	OcsbHitMod	Bidirectional	1
Reply Phase Signals			
Reply Status	OcsbRplySts[2:0]	Bidirectional	3
Destination Ready for Writes	OcsbDstnRdy	Bidirectional	1
Data Phase Signals			
Data Ready	OcsbDataRdy	Bidirectional	1
Data	OcsbData[255:0]	Bidirectional	256

MPOC On-Chip System Bus Signals

Fig. 4

Command Type	OcsbCmd[3:0]			
	3	2	1	0
Memory Instruction Read	0	0	0	0
Memory Data Read	0	0	0	1
Memory Read and Invalidate	0	0	1	0
Memory Write	0	0	1	1
I/O Read	0	1	0	0
I/O Write	0	1	0	1
Interrupt Acknowledge	0	1	1	0
Invalidate Acknowledge	0	1	1	1
Special Transactions	Reserved			

Command Types Defined by OcsbCmd[3:0] Signals

Fig. 5

Reply Type	OcsbRplySts[2:0]		
	2	1	0
Idle State	0	0	0
No Data Reply	0	0	1
Normal Data Reply	0	1	0
Implicit Writeback Reply	0	1	1
Retry Reply	1	0	0
Hard Failure Reply	1	0	1
Special Replies	Reserved		

Reply Types Defined by OcsbRplySts[2:0] Signals

Fig. 6

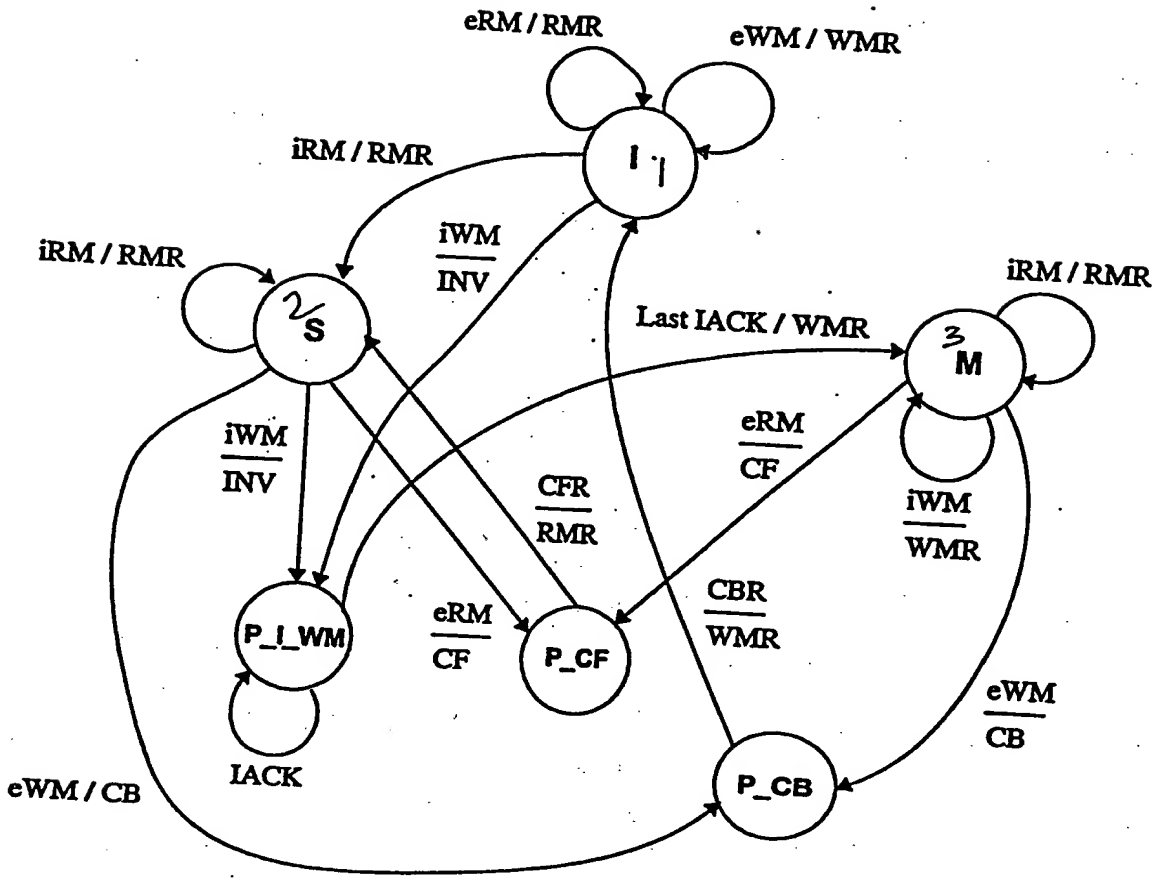
eRM / RMR
eWM / WMR
iRM / RMR
1
I
iRM / RMR
iWM
INV
2
S
iRM / RMR
Last IACK / WMR
3
M
iWM
INV
eRM
CF
CFR
RMR
iWM
WMR
P_I_WM
eRM
CF
P_CF
CBR
WMR
eWM
CB
IACK
eWM / CB
P_CB

Fig. 7